WHAT IS CLAIMED IS:

1. A solid state imager arrangement comprising: an image area, an output register which receives signal charge from the image area, a separate multiplication register into which signal charge from the output register is transferred, means for obtaining signal charge multiplication by transferring the charge through a sufficiently high field in elements of the multiplication register, and an additional register into which excess signal charge is transferred.

2. An arrangement as claimed in claim 1, wherein the excess signal charge is that exceeding a threshold level.

3. An arrangement as claimed in claim 2, wherein the threshold level is variable.

4. An arrangement as claimed in claim 1, wherein the excess signal charge is a percentage of the signal charge received from the image area.

5. An arrangement as claimed in claim 1, wherein excess signal charge is transferred to the additional register via one or more elements of the multiplication register.

6. An arrangement as claimed in claim 5, wherein excess signal charge is transferable from each element of the multiplication register to the additional register.

7. An arrangement as claimed in any of claims 1, wherein signal charge from the output register is applied to a separator which separates the excess signal charge from remaining signal charge, the excess charge being transferred to the additional register and the remaining signal charge to the multiplication register.

8. An arrangement as claimed in claim 1, wherein the multiplication register and additional register have the same number of elements.

9. An arrangement as claimed in claim 1 and wherein the amount of excess charge transferred to the additional register is determined by implanted barrier means.

10. An arrangement as claimed in claim 9, wherein the barrier means is located between the multiplication register and the additional register.

11. An arrangement as claimed in claim 1 and including gate means for controlling the transfer of excess signal charge to the additional register.

12. An arrangement as claimed in claim 1 and including means for combining signal charge after it has been transferred through the multiplication register with excess charge from the additional register.

13. An arrangement as claimed in claim 1, wherein signal charge multiplication is obtained in the additional register.

14. An arrangement as claimed in claim 1 and including a plurality of additional registers associated with the multiplication register.

15. An arrangement as claimed in claim 1, wherein a sufficiently high field region is obtained in each element of the multiplication register.

16. An arrangement as claimed in claim 1 and including means for synchronising signal readout from the multiplication register with line timing of a television rate signal.

17. An arrangement as claimed in claim 1, wherein signal charge is clocked through the multiplication register and excess charge through the additional register at the same rate as charge is clocked through the output register.

18. An arrangement as claimed in claim 1, wherein the amount of signal charge multiplication is controlled by controlling the amplitude of one or more drive pulses applied to a register to transfer signal charge therethrough.

19. An arrangement as claimed in claim 1, wherein the amount of signal charge multiplication is controlled by controlling the level of one or more dc potentials applied to a register.

20. An arrangement as claimed in claim 1, wherein the charge capacity of at least some of the elements of the multiplication register is larger than that of elements of the output register.

21. An arrangement as claimed in claim 1 and including a plurality of multiplication registers arranged to receive signal charge from the output register, at least one of the plurality having associated therewith an additional register.

22. A CCD imager comprising the solid state imager arrangement as claimed in claim 1.

23. A solid state imager arrangement comprising: an image area, an output register which receives signal charge from the image area, a multiplication register comprising a plurality of multiplication elements into which signal charge from the output register is transferred for charge multiplication, an additional register comprising additional elements arranged to receive excess signal charge from the multiplication register, and a clocking arrangement, wherein the clocking arrangement is arranged to clock the excess signal charge from the multiplication elements to corresponding ones of the additional elements.

24. An arrangement as claimed in claim 23, wherein the clocking arrangement comprises clocked wells arranged so that excess signal charge is transferred from the multiplication elements to the corresponding ones of the additional elements without charge from the additional elements returning to the multiplication elements.

25. An arrangement as claimed in claim 24, wherein the clocked wells are clocked by a clock source, the clock source also being arranged to clock the multiplication and/or the additional registers.